UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,057	10/09/2003	John W. Rapp	1934-14-3	3242

7590 11/14/2005	**EXAMINER**
Bryan A. Santarelli	FRANKLIN, RICHARD B
GRAYBEAL JACKSON HALEY LLP	

	ART UNIT	PAPER NUMBER
155-108th Avenue NE, Suite 350	2181	
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DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/684,057	RAPP ET AL.
	Examiner	**Art Unit**	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>06 September 2005</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-38</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-38</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>14 May 2004</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>4/11/05, 9/19/05</u>.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

1.   Claims 1 – 38 have been examined.

Election/Restrictions

2.   The Examiner has vacated the previous Office Action dated 08/02/2005. The restriction requirement presented in that Office Action is therefor withdrawn.

Drawings

3.   Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4.   The drawings are objected to because programming port 94a (Page 24, Line 15) is labeled 94 in Figure 6. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as

"amended." If a drawing figure is to be canceled, the appropriate figure must be

removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several

views of the drawings for consistency. Additional replacement sheets may be necessary

to show the renumbering of the remaining figures. Each drawing sheet submitted after

the filing date of an application must be labeled in the top margin as either

"Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are

not accepted by the examiner, the applicant will be notified and informed of any required

corrective action in the next Office action. The objection to the drawings will not be held

in abeyance.

Specification

5.   The disclosure is objected to because of the following informalities:

-        The references to applications filed on the same date of the current

         application lack application numbers and should be added or amended.

-        The reference to "Programmable Circuit And Related Computing Machine

         and Method (Attorney Docket No. 1934–14–3)" (Page 15 Lines 6 – 8) is a

         reference to the current application and should be removed or amended.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 1 – 2, 4 – 7, 9 – 12, 16, 20, 23, 30 – 33 are rejected under 35

U.S.C. 102(b) as being anticipated by Carmichael et al. US Patent No. 6,308,311

(hereinafter Carmichael).

As per Claims 1 and 30, Carmichael teaches a programmable circuit to receive

firmware that represents a configuration from an external source, store the firmware in a

memory (Figure 3 Item 36, Col 7 Lines 49 – 53), and download the firmware from the

memory (Col 7 Lines 58 – 60).

As per Claims 2 and 31, Carmichael teaches that the programmable circuit

operates in the configuration after downloading the firmware from the memory (Col 7

Lines 60 – 63).

As per Claim 4, Carmichael teaches that the programmable circuit has an

external memory (Fig 3 Items 36 or 38).

As per Claims 5 and 32, Carmichael teaches a programmable circuit and method

to download from a memory a first firmware that represents a first configuration (Col 6

Lines 27 – 35), operate in the first configuration, download from the memory a second

firmware that represents a second configuration (Col 7 Lines 58 – 60), and operate in

the second configuration (Col 7 Lines 40 – 65).

As per Claim 6, Carmichael teaches that the programmable circuit is operable to

receive the second firmware from an external source while operating in the first

configuration, and store the second firmware in the memory while operating in the first

configuration (Col 7 Lines 49 – 53).

As per Claims 7 and 16, Carmichael teaches a programmable circuit unit

comprising a memory (Figure 3 Item 36), a programmable circuit coupled to the memory

that can receive firmware that represents a configuration of the programmable circuit

from an external source (Col 7 Lines 40 – 65), store the firmware in a memory (Figure 3,

Col 7 Lines 49 – 53), and download the firmware from the memory (Col 7 Lines 58 –

60).

As per Claim 9, Carmichael teaches that the programmable-circuit unit comprises

a field-programmable gate array (FPGA) (Figure 3 Item 32).

As per Claims 10 and 20, Carmichael teaches a computing machine that

includes a processor (Figure 3 Item 34), and a programmable-circuit unit attached to the

processor that comprises a memory to store a first and second firmware that represents

a first and second configuration (Figure 3 Items 36 and 38) and can download from the

memory the first firmware (Col 6 Lines 27 – 35), operate in the first configuration,

download from the memory the second firmware in response to the processor (Col 7

Lines 58 – 60), and operate in the second configuration (Col 7 Lines 40 – 65).

As per Claim 11, Carmichael teaches that the second firmware is received from

an external source and stored in the memory while operating in the first configuration

(Col 7 Lines 49 – 53).

As per Claim 12, Carmichael teaches that the programmable-circuit unit can load

the second firmware while operating in the first configuration (Col 7 Lines 58 – 60).

As per Claim 23, Carmichael teaches that the computing machine processor can

send the second firmware to the programmable circuit, and that the programmable-

circuit can load the second firmware into the memory in response to the processor while

(Col 7 Lines 49 – 53).

As per Claim 33, Carmichael teaches sending the second firmware to the

programmable circuit, loading the second firmware into a memory with the

programmable circuit while the programmable circuit is operating in the first

configuration (Col 7 Lines 49 – 53), and downloading the second firmware from the

memory into the programmable circuit (Col 7 Lines 58 – 60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael) in view of RuDusky

US Patent Application Publication No. 2003/0061409 (hereinafter RuDusky).

As per claim 3, Carmichael teaches the programmable circuit with memory as

described per claim 1.

Carmichael does not teach that the memory is a non-volatile memory.

RuDusky teaches a programmable circuit that uses a non-volatile electrically

erasable and programmable read-only memory (EEPROM) to store configuration

information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to have modified Carmichael to include a non-volatile

memory to store configuration information.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to have modified Carmichael by the teaching of RuDusky because

using a non-volatile memory to store configuration information would allow for the

configuration information to remain in the memory even with no power to the system.

As per claim 8, Carmichael teaches the programmable circuit with memory as described per claim 7.

Carmichael does not teach that the memory is an EEPROM.

RuDusky teaches a programmable circuit that uses an EEPROM to store configuration information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Carmichael to include an EEPROM to store configuration information.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Carmichael by the teaching of RuDusky because using an EEPROM to store configuration information would allow for the configuration information to remain in the memory even with no power to the system.

8.   Claims 13 – 15, 17 – 18, 24, 27 – 29, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carmichael et al. US patent No. 6,308,311 (hereinafter Carmichael) in view of Erickson et al. US Patent Application Publication No. 2003/0177223 (hereinafter Erickson).

As per claim 13, Carmichael teaches a programmable-circuit unit that includes a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); and a first programmable circuit coupled to the memory and operable to download a first configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the

first configuration, download a second configuration from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the second configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the memory and first programmable circuit that is operable to download a third firmware from the memory, operate in the third configuration, download a fourth firmware from the memory, and operate in the fourth configuration.

Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or field programmable gate arrays (FPGAs) (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Carmichael to include multiple FPGAs that run different versions of firmware that is updated.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Carmichael by the teaching of Erickson because including multiple FPGAs that run different versions of firmware that is updated allows firmware to be changed in a system with higher computing power than a single FPGA system.

As per claim 14, Carmichael as modified teaches receiving the second

configuration from an external source while operating in the first configuration and

storing the second configuration in the memory while operating in the first configuration

(Carmichael; Col 7 Lines 49 – 53).

As per claim 15, Carmichael as modified teaches that the programmable-circuit is

a FPGA (Carmichael; Figure 3 Item 32).

As per claim 17, Carmichael teaches the computing machine with a processor

coupled to a programmable-circuit unit as described per claim 16.

Carmichael does not teach determining whether the firmware is already stored in

the memory before sending the firmware to the programmable circuit, and sending the

firmware to the programmable circuit only if the firmware is not already stored in the

memory.

Erickson teaches determining if a firmware is stored in a memory coupled to the

programmable circuit (Erickson; Figure 3 Items 320 – 360) and only sending the

firmware to the programmable circuit if the second firmware is not stored in the memory

(Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Carmichael to include the checking to see if the

firmware is already stored in the memory and not sending the firmware if it is already

stored.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Carmichael by the teaching of Erickson to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored because this reduces the chance of sending data that has already been sent and thereby wasting processing power on a data transfer that is not needed.

As per claim 18, Carmichael as modified teaches a configuration registry (Erickson; Figure 1 Items 130 and 140) that stores firmware (Erickson; Figure 1 Item 132, Paragraph [0014]) and indicates that the firmware represents a desired configuration (Erickson; Paragraph [0015]), and that the processor is operable to download the firmware from the configuration registry into the programmable circuit (Erickson; Paragraph [0017] Lines 9 – 13).

As per claim 24, Carmichael teaches a programmable-circuit unit that has a processor (Carmichael; Figure 3 Item 34); a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); and a first programmable circuit coupled to the memory and operable to download a first configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the first configuration, download a second configuration from the memory in response to the processor (Carmichael; Col 7 Lines 58 – 60), and operate in the second configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the

memory and the first programmable circuit that is operable to download a third firmware

from the memory, operate in the third configuration, download a fourth firmware from

the memory in response to the processor, and operate in the fourth configuration.

Erickson teaches a system that has multiple processors (Erickson; Figure 1

Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running

different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware

running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Carmichael to include multiple FPGAs that run

different versions of firmware that is updated.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to have modified Carmichael by the teaching of Erickson because

including multiple FPGAs that run different versions of firmware that is updated allows

firmware to be changed in a system with higher computing power than a single FPGA

system.

As per claim 27, Carmichael as modified teaches receiving the second

configuration from an external source and storing it in memory while operating in the

first configuration (Carmichael; Col 7 Lines 49 – 53).

As per claim 28, Carmichael as modified teaches a separate memory unit to hold

firmware information for each processor (Erickson; Figure 1 Items 120 and 122).

As per claim 29, Carmichael as modified obviously teaches that the separate

memories are disposed on separate integrated circuits because putting memories on

different integrated circuits would be an obvious engineering choice (See *In re Larson*,

340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); *In re Wolfe*, 251 F.2d 854, 855,

116 USPQ 443, 444 (CCPA 1958)).

As per claim 34, Carmichael teaches the method as described per claim 32 and

loading the second firmware into the memory with the programmable circuit while

operating in the first configuration (Carmichael; Col 7 Lines 58 – 60) and downloading

the second firmware from the memory into the programmable circuit (Carmichael; Col 7

Lines 40 – 65)

Carmichael does not teach determining if the second firmware is stored in a

memory coupled to the programmable circuit and sending the second firmware to the

programmable circuit only if the second firmware is not stored in the memory.

Erickson teaches determining if the second firmware is stored in a memory

coupled to the programmable circuit (Erickson; Figure 3 Items 320 – 360) and only

sending the second firmware to the programmable circuit if the second firmware is not

stored in the memory (Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Carmichael to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Carmichael by the teaching of Erickson to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored because this reduces the chance of sending data that has already been sent and thereby and wasting processing power on a data transfer that is not needed.

As per claim 36, Carmichael teaches a first programmable circuit coupled to a memory and operable to download a first configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the first configuration, download a third configuration from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the third configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the memory and the first programmable circuit that is operable to download a second firmware from the memory, operate in the second configuration, download a fourth firmware from the memory, and operate in the fourth configuration.

Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running

different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware

running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Carmichael to include multiple FPGAs that run

different versions of firmware that is updated.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to have modified Carmichael by the teaching of Erickson because

including multiple FPGAs that run different versions of firmware that is updates allows

for firmware to be changed in a system with higher computing power than a single

FPGA system.

9.   Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael) in view of

Hartmann US Patent No. 6,096,091 (hereinafter Hartmann).

As per claim 19, Carmichael teaches the computing machine with a processor

coupled to a programmable-circuit unit as described per claim 16.

Carmichael does not teach that the programmable-circuit unit comprises a

pipeline unit, and that the programmable circuit includes a hardwired pipeline that can

operate on data.

Hartmann teaches the use of a reconfigurable programmable circuit unit that

includes a pipeline unit (Hartmann; Figure 2, Col 2 Lines 32 – 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Carmichael to include a pipeline unit.

It would have been obvious to one of ordinary skill in the art at the time of

invention to modify Carmichael by the teaching of Hartmann because adding a pipeline

unit would speed up data processing of the system.

10.   Claims 21 – 22, and 35 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael)

in view of Moore US Patent No. 6,893 873 (hereinafter Moore).

As per claim 21, Carmichael teaches the computing machine as described per

claim 20.

Carmichael does not teach that the processor has a first test port, the

programmable circuit has a second test port coupled to the first test port, and the

processor is able to load the first firmware into memory via the first and second test

ports.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C

Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308,

Col 5 Lines 28 – 31) and can send the result to a processor through the test ports

(Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory

through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6

Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Carmichael to include the test ports and data

transfer through the test ports.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Carmichael by the teaching of Moore because the use of

test ports and the self test eases the burden on a tester machine (Moore; Col 5 Lines 43

– 45).

As per claim 22, Carmichael as modified teaches that the processor comprises a

first test port, the programmable-circuit unit comprises a second test port that is coupled

to the first test port (Moore; Figures 2A – 2C Item 206), the programmable circuit can

perform a self-test and send self-test data to the processor via the first and second test

ports (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31), and firmware is then loaded into

a memory through the test ports if the self-test results are appropriate (Moore; Figure

2C, Col 6 Lines 4 – 13).

As per claim 35, Carmichael teaches the method as described per claim 32.

Carmichael does not teach that operating the programmable circuit in the first

configuration comprises testing the programmable circuit, and downloading the second

firmware comprises downloading the second firmware only if the programmable circuit

passes testing.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C

Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308,

Col 5 Lines 28 – 31) and can send the result to a processor through the test ports

(Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory

through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6

Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Carmichael to include the test ports, self-test,

and data transfer through the test ports only if a certain test result was discovered.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Carmichael by the teaching of Moore because the use of

test ports and the self test eases the burden on a tester machine (Moore; Col 5 Lines 43

– 45).

11.   Claims 25 – 26, and 37 – 38 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Carmichael et al. US Patent No. 6,308,311 (hereinafter Carmichael)

in view of Erickson et al. US Patent Application Publication No. 2003/0177223

(hereinafter Erickson) as applied to claims 13 – 15, 17 – 18, 24, 27 – 27, 34, and 36

above, and further in view of Moore US Patent No. 6,893,873 (hereinafter Moore).

As per claim 25, Carmichael as modified by Erickson teaches a computing

machine with multiple programmable circuits as described per claim 24.

Carmichael as modified by Erickson does not teach that the processor has a first test port, the programmable circuit has a second test port coupled to the first test port, and the processor is able to load the first and third firmware into memory via the first and second test ports.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Carmichael as modified by Erickson to include the test ports, self-test, and data transfer through the test ports only if a certain test result was discovered.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Carmichael as modified by Erickson by the teaching of Moore because the use of test ports and the self test eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 26, Carmichael as modified by Erickson and further modified my Moore teaches the first and second programmable circuits to perform self-tests (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and provide the self-test data to the processor

via the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67), and then each programmable

circuit loads a different firmware if the self-test data indicate a predetermined result of

the self-tests (Moore; Figure 2C, Col 6 Lines 4 – 13).

As per claim 37, Carmichael as modified my Erickson teaches a method

including multiple programmable circuits as described per claim 36.

Carmichael as modified by Erickson does not teach wherein downloading the first

and second firmware comprises downloading the first and second firmware into the first

and second programmable circuits via a test port.

Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C

Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308,

Col 5 Lines 28 – 31) and can send the result to a processor through the test ports

(Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory

through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6

Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Carmichael as modified by Erickson to include

the loading of firmware though test ports.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Carmichael as modified by Erickson by the teaching of

Moore because the use of test ports eases the burden on a tester machine (Moore; Col

5 Lines 43 – 45).

As per claim 38, Carmichael as modified by Erickson and further modified by

Moore teaches testing the first and second programmable circuits (Moore; Figure 3 Item

308, Col 5 Lines 28 – 31), and wherein loading the firmware into the programmable

circuits comprises loading the firmware only if the testing indicates that the

programmable circuit is functioning as desired (Moore; Figure 2c, Col 6 Lines 4 – 13).
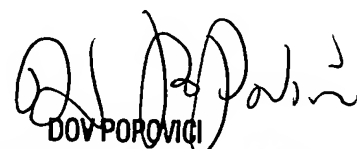

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Richard Franklin whose telephone number is (571) 272-

0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Richard Franklin
Patent Examiner

DOV POPOVICI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100